

## Nanofabrication using a stencil mask

Mandar M. Deshmukh, D. C. Ralph,<sup>a)</sup> M. Thomas, and J. Silcox  
*Cornell University, Ithaca, New York 14853*

(Received 5 May 1999; accepted for publication 20 July 1999)

We describe tests of a technique to fabricate nanostructures by the evaporation of metal through a stencil mask etched in a suspended silicon nitride membrane. Collimated evaporation through the mask gives metal dots less than 15 nm in diameter and lines 15–20 nm wide. We have investigated the extent of hole clogging and the factors which determine the ultimate resolution of the technique.

© 1999 American Institute of Physics. [S0003-6951(99)00437-4]

The usual procedures for fabricating nm-scale devices, using electron-beam, x ray, or other forms of lithography, involve exposing a pattern in a polymer-resist layer applied directly to a sample substrate. However, there exist several circumstances in which it would be convenient to do away with the resist on the sample; instead completing the pattern formation process separately to make a free-standing stencil, which is later used to deposit patterned material onto the substrate. By this means, lithography could be performed on substrate materials which would be damaged by the chemical or thermal stresses encountered during resist application and baking. Another application is for the fabrication of nanostructures on ultrahigh vacuum surfaces, for experiments such as studies of atomic diffusion, or the fabrication of electrodes to contact self-assembled nanostructures. It would also be possible to make devices on unusual substrates, for which it is not possible to achieve the uniform coating of resist necessary for ordinary processing. We have in mind the desire to write nm-scale devices directly on the tips of scanning probe microscopes, for the purpose of creating new types of scanning sensors.<sup>1</sup>

In this letter, we describe a process for fabricating nanostructures by evaporating metal through holes in a suspended silicon nitride membrane. In doing this work we follow many groups who have used stencil techniques to make structures  $\geq 0.1 \mu\text{m}$  in scale.<sup>2–4</sup> We are able to write metal dots 15 nm in diameter and lines 15–20 nm wide. We have also tested the rate at which nm-scale holes in the stencil clog during the deposition process, and the extent to which the ultimate resolution of this technique is limited by the divergence angle of the deposition beam and diffusion of atoms on the sample surface.

The stencil masks are made by adapting a procedure used previously for fabricating metal point contacts<sup>5</sup> and tunneling devices.<sup>6</sup> First, low-stress silicon nitride is deposited on both sides of a  $\langle 100 \rangle$  double-side-polished silicon wafer. Photolithography and etching in an aqueous KOH solution are used to remove selected regions of the silicon to leave square suspended membranes of silicon nitride 50 nm thick and 60–80  $\mu\text{m}$  on a side. Electron-beam lithography is then performed to write an array of holes on the membrane, using the Leica VB6 at the Cornell Nanofabrication Facility, operating at 100 keV. After development, the holes are etched

through the silicon nitride membrane using a  $\text{CHF}_3/\text{O}_2$  plasma. The etching conditions are such that the hole is bowl shaped, and the final orifice is smaller than the original pattern formed by lithography.<sup>5</sup> Figure 1(a) displays a scanning transmission electron microscope (STEM) bright-field image of a single 5-nm-diam hole in an array, looking through the membrane. The gradual darkening in the region surrounding the hole is due to the taper on the sides of the bowl-shaped hole. In our tests we have used holes ranging up to 50 nm in diameter, and also larger orifices for contact pads and other test structures.

The geometry for deposition through the stencil mask is shown in Fig. 2. For simple single-step metal depositions, the mask can be clamped directly to a substrate. However, we find that the mask-substrate spacing in this case varies, due to small particulates or surface irregularities, typically being in the range of 1  $\mu\text{m}$ . A predictable spacing is necessary for alignment of multiple-angle evaporations and for tests of the ultimate size resolution of the technique, so we introduce 1.6- $\mu\text{m}$ -diam silica spheres<sup>7</sup> as spacers between

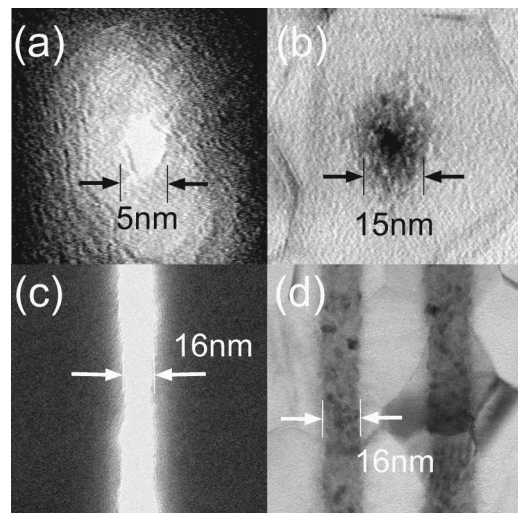


FIG. 1. Bright-field STEM images. (a) A hole 5 nm in diameter etched through a silicon nitride membrane. (b) A metal dot made by evaporating 10 nm of Er through an orifice 5–10 nm in diameter onto an oxidized aluminum film held at room temperature. (c) Section of a 4  $\mu\text{m}$ -long  $\times$  15–20-nm-wide line etched through a silicon nitride membrane. (d) Sections of 10-nm-thick Er lines which are deposited through an orifice similar to the one shown in (c), at room temperature onto an oxidized Al film. The two lines, 19 nm and 16 nm wide, were made by separate depositions of Er, from different angles, through the same linear hole.

<sup>a)</sup>Electronic mail: ralph@msc.cornell.edu

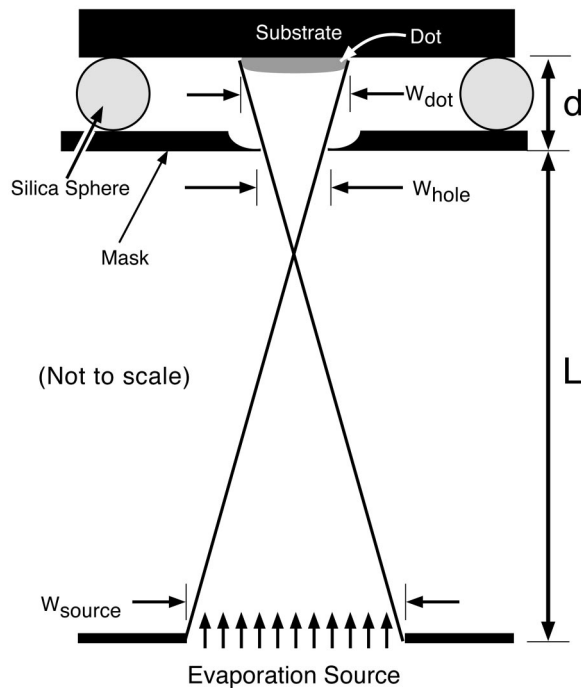


FIG. 2. Diagram of deposition through the stencil mask using a pinhole evaporation source. (Not to scale).

the stencil and substrate before clamping. The sample/stencil assembly is attached to a stepper-motor controlled tilting stage within an evaporator, so that the angle of evaporation can be varied. The mask-substrate spacing with the microspheres is generally reproducible to  $\pm 0.1 \mu\text{m}$ , and is checked by evaporating metal through a nanohole from two known angles, measuring the distance between the resulting dots on the substrate by scanning electron microscopy (SEM) or atomic force microscopy (AFM), and using triangulation. The sample and stencil are baked in vacuum to remove adsorbed water before the evaporation (one exception will be noted).

In order to produce nm-scale features by deposition through a stencil more than  $1 \mu\text{m}$  from the substrate, the incoming beam of metal atoms must be collimated. This is achieved by using a resistive-heating source containing a pinhole of width  $w_{\text{source}} = 1 \text{ mm}$  through which metal is evaporated.<sup>8</sup> From the geometry shown in Fig. 2, assuming no diffusion of atoms on the surface, the width of a deposited dot should be  $w_{\text{dot}} \approx w_{\text{hole}} + (d/L)w_{\text{source}}$ , where  $w_{\text{hole}}$  is the width of the orifice in the stencil,  $d$  is the stencil-substrate spacing, and  $L = 30 \text{ cm}$  is the source-stencil spacing.<sup>9</sup> The broadening  $(d/L)w_{\text{source}}$  is therefore expected to be approximately  $5 \text{ nm}$ .

Figure 1(b) shows a bright-field plan-view STEM image of one example from an array of metal dots made by depositing  $10 \text{ nm}$  of erbium (Er) through an orifice  $5\text{--}10 \text{ nm}$  in diameter onto a room temperature substrate. The deposited dot is  $\sim 15 \text{ nm}$  in diameter. The substrate in Fig. 1(b) [and also Fig. 1(d)] is an oxidized Al film,  $30 \text{ nm}$  thick, deposited on a photoresist layer on top of a Si wafer. This geometry allows the Al film to be lifted off for STEM examination of the Er structures. Because of the photoresist layer, the samples in Fig. 1 were not baked prior to the deposition. The images are taken looking through the Al film, whose grains

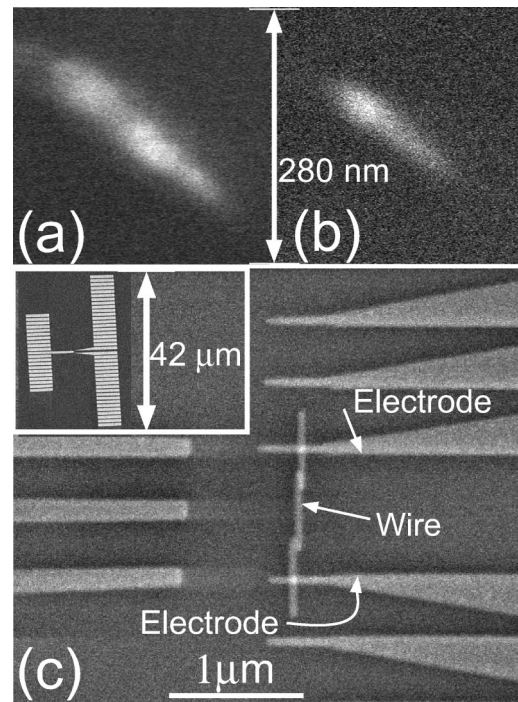


FIG. 3. (a) and (b) Clogging tests: SEM images of Er deposited through 40 and 20-nm-diameter orifices onto oxidized Si, as the substrate was gradually tilted so as to scan the deposition spot. The hole clogs after the deposition of  $65 \text{ nm}$  and  $30 \text{ nm}$  of material respectively. (c) 25-nm-wide, 10-nm-thick Er line connected to macroscopic electrodes using multiple-angle evaporations. The inset shows the pattern of the stencil mask used to fabricate the device.

are visible on the  $40\text{--}50 \text{ nm}$  scale. We choose Er for deposition tests due to its sticking properties, good visibility in electron microscopes (atomic number = 68), and convenient melting temperature. Chromium and aluminum have also been deposited successfully. We have verified that the dots are Er, using electron energy-loss spectroscopy.

In Fig. 1(c), we show a section of a  $4\text{-}\mu\text{m}$ -long line-shaped orifice in a stencil membrane, and in Fig. 1(d) images of two  $10\text{-nm}$ -thick Er lines deposited through such a hole. Both the deposited lines and the stencil orifice have widths  $15\text{--}20 \text{ nm}$ . The grain size of the deposited Er is visible in Fig. 1(d),  $2\text{--}5 \text{ nm}$ .

We have investigated how much material may be deposited through the nm-scale holes before they become clogged. This test is done by slowly tilting the stencil/substrate assembly, using a stepper motor, while Er is evaporated at a constant rate so as to draw a line of material on the substrate. In one test, with a  $1.8\text{-}\mu\text{m}$  stencil-substrate spacing, we deposited  $200 \text{ nm}$  of Er over the course of a  $20^\circ$  rotation, which in the absence of hole-clogging would give a  $660 \text{ nm}$  line. The deposited structures [e.g., Figs. 3(a) and 3(b)] have an angular shape, thinning as the evaporation proceeds, indicating that the holes close gradually. From the length of the lines, we can estimate that for a hole of approximately  $40 \text{ nm}$  diameter,  $65 \text{ nm}$  of evaporated Er clogs the hole, while for  $20\text{-nm}$ -diam holes,  $30 \text{ nm}$  of Er is the limit. Somewhat greater thicknesses of gold can be deposited without clogging the stencil, approximately 3 times the hole diameter; however gold produces broader deposited features than Er due to increased surface diffusion.

As a test of the extent to which the divergence of the

TABLE I. AFM study of the thicknesses of Er dots deposited through orifices of varying diameter, in order to measure the spreading of the deposited Er. Room-temperature and 77 K depositions were performed through the same sets of holes, from different angles. The smaller hole sizes listed for the 77 K deposition reflect partial hole clogging. The uncertainties are standard deviations for dots deposited through different holes of similar size in the same array. Diameters are accurate to  $\pm 3$  nm.

Hole diameter(nm)	500	47	31	25
Height for RT (nm)	$10.8 \pm 0.1$	$10.4 \pm 0.3$	$8.5 \pm 0.1$	$6.6 \pm 0.3$
Hole diameter (nm)	500	41	25	19
Height for 77 K (nm)	$10.1 \pm 0.1$	$10.9 \pm 0.3$	$10.4 \pm 0.4$	$7.3 \pm 0.2$

incident atom beam and also surface diffusion of Er limit the resolution of the stencil technique, we have used AFM to compare the heights of Er dots with different diameters, deposited simultaneously at fixed angle onto oxidized silicon through holes in one stencil membrane. The heights are listed in Table I as averages over tens of dots made in arrays of similar diameters. The total deposited thickness of Er is determined by measuring the thickness of very large (0.5- $\mu\text{m}$ -wide) features in the test array. Smaller-diameter dots are progressively shorter, as would be expected due to spreading of the deposited metal. In order to obtain an approximate measure of this spreading, we can model the deposited features as pillars (slightly tapered to take into account hole clogging) convolved with a Gaussian spreading function. This is not accurate in all cases, since some dots are observed with thicknesses greater than the deposited film, due to clustering of the metal. However, the average dot heights indicate a full width at half maximum (FWHM) for the spreading function of approximately  $18 \pm 5$  nm. For a substrate cooled to liquid nitrogen temperature during the evaporation, this is reduced to  $10 \pm 4$  nm, so we can conclude that thermal diffusion of Er contributes to the spreading at room temperature.

In order to make use of nm-scale structures as electrical devices, it is necessary to connect them to macroscopic leads. We have accomplished this by making a stencil pat-

tern which contains both a line on the 25-nm scale and electrodes on the 10's-of- $\mu\text{m}$  scale. Then we have connected the wire and the electrodes using a series of three 10-nm-thick Er evaporations from different angles [Fig. 3(c)]. The room-temperature resistance of the wire+electrodes shown in Fig. 3(c) is 1000  $\Omega$ .

In summary, we have developed a technique for fabricating metal structures approximately 15–20 nm wide using a stencil mask. Structures can be made by evaporating metal at multiple fixed angles, or they can be drawn continuously by tilting the stencil and thus scanning the substrate relative to the stencil orifice. The technique is useful for performing lithography on substrates for which it is not possible to apply resist.

The authors thank C. T. Black, who originated the idea for this work. They also acknowledge helpful discussions with S. Guéron, J. A. Katine, E. B. Myers, A. Pasupathy, and J. R. Petta, and we thank D. W. Carr, G. Comeau, and R. C. Tiberio for technical help. The work was supported by the Research Corporation, the Packard Foundation and the NSF (DMR-9705059). A portion of the work was performed at the Cornell node of the National Nanofabrication Users Network, funded by the NSF. The STEM Facility is supported by the NSF through the Cornell Center for Materials Research.

<sup>1</sup>M. J. Yoo, T. A. Fulton, H. F. Hess, R. L. Willett, L. N. Dunkleberger, R. J. Chichester, L. N. Pfeiffer, and K. W. West, *Science* **276**, 579 (1997).

<sup>2</sup>K. Ono, H. Shimada, S. Kobayashi, and Y. Ootuka, *Jpn. J. Appl. Phys., Part 1* **35**, 2369 (1996).

<sup>3</sup>J. N. Ullom, P. A. Fisher, and M. Nahum, *Phys. Rev. B* **58**, 8225 (1998).

<sup>4</sup>C. Stamm, F. Marty, A. Vaterlaus, V. Weich, S. Egger, U. Maier, U. Ramsperger, H. Fuhrmann, and D. Pescia, *Science* **282**, 449 (1998).

<sup>5</sup>K. S. Ralls, R. A. Buhrman, and R. C. Tiberio, *Appl. Phys. Lett.* **55**, 2459 (1989).

<sup>6</sup>D. C. Ralph, C. T. Black, and M. Tinkham, *Phys. Rev. Lett.* **74**, 3241 (1995).

<sup>7</sup>Duke Scientific Corp., Palo Alto, CA 94303.

<sup>8</sup>R. D. Mathis Company, Long Beach, CA 90806.

<sup>9</sup>C. T. Black, Ph.D. thesis, Harvard University, 1996.