DATA CONVERSION PRINCIPLES

Chapter 2

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Chapter 2

DATA CONVERSION PRINCIPLES

2.1 INTRODUCTION

Measuring instruments perform the function of converting the value of a parameter under measurement into that of a second analogous parameter which is easy to display and read. For example, a mercury thermometer converts temperature into the length of a column of mercury. Most panel instruments convert the parameters being measured into the angle of deflection of a pointer on a dial: e.g. the time of the day, the speed of an automobile or the weight of a person. All these are examples of analog instruments: the parameter being measured is expressed or displayed in terms of an analogous parameter.

Ideally, the relationship between the measured parameter and the parameter being displayed should be linear. This, however, is not always the case. For example, let us consider ceramic resistance elements used for electronic temperature measuring instruments. Here the resistance varies nonlinearly with temperature. In one case the resistance is 100 ohms at 0°C, 103.90 ohms at 10°C, 107.79 ohms at 20°C, etc.

Control instruments use the value of a control parameter (e.g. the angle of rotation of a pressure valve control or of a variable potentiometer) to effect a corresponding variation in the parameter being controlled (e.g. the rate of gas flow or the gain of an amplifier).

In physical systems, the values of such parameters vary continuously over a finite range. It therefore seems natural to perform measurement and control using analog instruments such as the ones mentioned above.

Measurement and control can also be accomplished using digital systems i.e. systems where parameters are represented as numbers.

2.1.1 Representation of Information in Digital Systems

Numbers can be represented in a digital system as they are on paper:
as sequences of digits, using an appropriate number system. The decimal number system which is commonly in use, has a total of ten symbols (the digits 1 to 9 and 0) and the base of the system is ten. A number in the decimal number system (a decimal number) can be expanded as a sequence of powers of ten.

e.g.

\[ 963 = 9 \times 10^2 + 6 \times 10^1 + 3 \times 10^0 = 900 + 60 + 3 \]

\[ .104 = 1 \times 10^{-1} + 0 \times 10^{-2} + 4 \times 10^{-3} = \frac{1}{10} + \frac{0}{1000} + \frac{4}{10000} \]

To represent numbers in circuits using the decimal number system is rather involved. For simplicity, digital circuits use the binary number system which has only two symbols (0 and 1). Consequently, the base of this system is two. A number in the binary system (a binary number) can be expanded as a sequence of powers of two. There are fairly simple ways of converting numbers from one number system to another, e.g. as shown below (here, the subscripts indicate the radix of the number system used).

\[ (1011)_2 = 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \]

\[ = 8 + 0 + 2 + 1 = (11)_10 \]

\[ (.101)_2 = 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} \]

\[ = \frac{1}{2} + \frac{0}{4} + \frac{1}{8} = \frac{5}{8} = (.625)_10 \]

A binary digit (or bit) can be represented as a voltage level on a wire. The standard voltage levels used for the TTL (Transistor Transistor Logic) family of Integrated Circuits are 0 volts for Zero and 5 volts for One. A bistable circuit can also be used to represent and store one bit, one of the two possible states representing a zero and the other, a one.

To represent and store a binary number several bits long, one would need a number of bistable elements, one per bit stage. Input and output of numbers, similarly, requires several signal wires, one per bit. This is the so called parallel representation of digital data,
because individual bits are represented in parallel using several bistables or signal wires. In a serial system of representation, a single bistable element or wire is used to represent several bits in sequence, one after the other.

2.1.2 The Need for Analog to Digital and Digital to Analog Conversion:

Usage of digital system for measurement and control usually requires conversion of continuously varying measured parameters into proportional numbers and numbers denoting control variables into proportional physical (usually voltage or current) signals. Units which perform these functions are termed Analog to Digital (A/D) and Digital to Analog (D/A) Converters respectively.

This round about process (involving conversion into a digital mode of representation and back again into analog form) remains advantageous for several reasons:

1. Digital signals are much more convenient to store and retrieve, than their analog counterparts.
2. Digital data, unlike analog signals, can be stored, processed or transmitted over long distance without corruption, even in the presence of considerable noise. This is because in case of analog operation, information is represented directly as the magnitude of a voltage or a current signal. The signal at every instant has therefore to be represented accurately. Any noise in this signal will reflect as a corresponding error in representation; e.g. a voltage of 0.75V on a wire may represent the number 0.75. If there is noise of 150 mV on the wire, this will cause an error of 20% in reading the number. On the other hand, digital signals can assume only two values corresponding to a 0 or a 1 say, 0 volts or 5 volts respectively. Let us say the same number is represented as the binary fraction 0.110 on three wires. The voltage levels on these wires will be 5V, 5V and 0V respectively. Even with a noise of 1V on each of these wires, there will be no confusion or error, if the circuitry is suitably designed.
3. There are reasonably simple techniques for detection and correction of errors that might occur in the course of storage, retrieval and transmission of digital data.
2.2 DIGITAL TO ANALOG CONVERSION:

A wire wound potentiometer or rheostat used in a college laboratory is a good model of a digital to analog (D/A) converter (Fig. 2.1). Let us assume that it has \( n \) turns of wire and that the sliding wiper (whose movement varies the resistance) is attached to a pointer moving on a graduated scale with \( n \) equal divisions. Let the total resistance of the potentiometer be \( R \) and the voltage applied across it be \( V \).

To convert a digital number \( K \) into the corresponding analog voltage, the pointer is placed at the point marked \( K \) on the scale. It is quite easy to see that the output voltage is

\[
\frac{V}{R} \cdot \frac{K}{n}
\]

In this example, we took an integer for conversion. It is common to use proper fractions rather than integers as inputs. This can be easily accomplished in the above case by suitably marking the scale, such that the maximum corresponds to unity and the other divisions represent suitable decimal or binary fractions. In that case, for a fraction \( D = \frac{K}{n} \) as input, the output voltage will be

\[
A = \frac{V}{R} \cdot D \quad (1)
\]

2.2.1 Basic Concepts in D/A Conversion

Transfer Function: A D/A Converter accepts a given digital number \( D \) as input and converts it into a proportional voltage or current signal \( A \) which is made available as output. For this, it requires a reference voltage \( V_R \) as input.
Data Conversion Principles

Fig. 2.2 represents a block diagram of a typical D/A Converter.

![Block Diagram of a D/A Converter](image)

**Fig. 2-2 Block Diagram of a D/A Converter**

The digital input \( D \) (the sequence of digits \( a_1, \ldots, a_n \)) is normally expressed as a proper fraction. Here, the decimal point is taken to be at the extreme left of the sequence.

In a general case, where \( r \) is the radix of the number system,

\[
D = a_1 r^{-1} + a_2 r^{-2} + \ldots + a_n r^{-n} \quad (2)
\]

The analog output \( A \) is given by

\[
A = V_R \cdot D \quad (3)
\]

From (2) and (3),

\[
A = V_R \cdot (a_1 r^{-1} + a_2 r^{-2} + \ldots + a_n r^{-n}) \quad (4)
\]

For the binary system which is commonly used in computers, \( r \) is 2. Each of the coefficients \( a_i \) is either a zero or a one. Hence,

\[
A = V_R \cdot (a_1 2^{-1} + a_2 2^{-2} + \ldots + a_n 2^{-n}) \quad (5)
\]

Equation (5) defines the basic transfer function for any D/A Converter. For example, a fractional digital input 0.101 (assuming 3 bit D/A conversion and a reference voltage of 10 volts) will yield
(using eqn (5)),

\[ A = 10 \left( 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} \right) \]

\[ = 10 \left( \frac{1}{2} + \frac{1}{8} \right) = \frac{59}{8} = 6.25 \text{ volts.} \]

Fig. 2.3 shows the transfer function for a 3 bit binary D/A Converter. It accepts digital inputs ranging from \(0.000\) to \(0.111\)

i.e. \(0, \frac{1}{8}, \frac{2}{8} \ldots \frac{7}{8}\).

The corresponding analog output in each case is indicated on the \(y\) axis.

It can be seen that the maximum input (when all bits have the value 1, in this case, 111) does not give rise to the full scale analog value. Using equation 3, the corresponding output is given by

\[ A = R(1 - 2^{-n}) \]

\[ = R(1 - x^{-n}) \quad \text{for} \quad x = 2 \]

\[ \ldots \quad (6) \]

\[ \text{Fig. 2.3 Transfer Function of D/A Converter} \]
For a value \( R = 10 \) volts and \( n = 3 \)

\[
A = 10 (1 - 2^{-3}) = 10 (1 - \frac{1}{8}) = 10 \times \frac{7}{8} = \frac{70}{8}
\]

\[= 8.75 \text{ volts.}\]

This analog output falls short of the full scale value by \( 10 \times \frac{1}{8} \) volts i.e. 1.25 volts.

2.2.2 Direct D/A Converters

**Weighted Resistor D/A Converter:**

To arrive at the magnitude of a number, one has to total the contribution of individual bits with due weightages (e.g. the number \( 0.10101 \) is \( \frac{1}{2} + \frac{0}{4} + \frac{1}{8} + \frac{0}{16} + \frac{1}{32} = \frac{21}{32} \)).

A D/A converter performs the same operation with analogous physical entities. The most common method is summation of proportional electrical currents. A direct parallel D/A Converter accepts \( n \) parallel inputs, \( D \) (Fig. 2.4). Each \( i^{th} \) input has to switch a current of magnitude \( I \times 2^{-i} \) into a summing operational amplifier. It does this by switching an input resistor of value \( R \times 2^i \) between a voltage \( V_R \) and ground, depending on whether the corresponding bit is 1 or 0. The total current fed to the operational amplifier will therefore be proportional to the value of the number at the input of the converter.

In Fig. 2.4, choosing a reference voltage \( V_R = 10V \) and \( R = 10K \) ohms will generate a current \( I = 1mA \) in the most significant bit (MSB) position. Since the operational amplifier is working in the low output impedance current-to-voltage converter mode, a current \( I \) of 1 mA at the input will generate a voltage shift of 5 volts at the output if the feedback resistor \( R_F \) is 5K ohms. The next bit will cause a shift of 2.5 volts and so on.

The advantage of this type of D/A Converter is that only one resistor is required per bit. However, the resistors span a very wide range of values. Consider, for example, a 12 bit D/A Converter. If the value of the resistor chosen for the MSB position is 10K ohms, then the resistor in the least significant bit (LSB) position has to be 10K \( (2^{11} - 1) \), i.e. 20.48 megohms. Exact matching of resistor values becomes very difficult over such a wide range.

The overall accuracy of this type of D/A Converter depends on the quality of the switches, resistors and the amplifier. The conversion
speed is limited by the turn-on and turn-off times of the switches, the parasitic reactances of the resistors and the slewing rate of the operational amplifier.

Resistor-Ladder D/A Converter:

The main disadvantage of the circuit of Fig. 2.4 (Parallel D/A Converter with weighted resistor) is the need for a wide range of resistor values.

The resistor-ladder D/A Converter of Fig. 2.5 overcomes this problem; it uses only two values of resistors per bit position. Since the values of the chosen resistors are only two and close to each other (R and 2R), matching resistor values and temperature coefficients becomes easy.

In the resistor-ladder D/A Converter (Fig. 2.5) each input resistor is connected either to the reference voltage or ground
Fig. 2-5  Resistor Ladder D/A Converter
depending on the value of the corresponding bit. To understand its operation, let us consider the equivalent circuit of the ladder network. All resistors of the ladder are effectively connected to ground. (The input of the operational amplifier is virtual ground and the switches have zero output impedance).

Assume bit \( i \) is one and all others zero. Switch \( i \) is then connected to voltage \( V_R \) and all others are at ground. Let a current \( I \) flows into the switch.

We can easily verify that the impedance at any of the nodes \( N_i \) to \( N_{i+1} \) looking from the left, is \( R \). This can be seen to be true for node \( N_1 \) (consider the inner most box \( B_1: 2R/2R = R \)). The same is true for \( N_2 \) (consider box \( B_2 \) where again, \( 2R/2R = R \)) \( N_2 \) and so on for any \( N_i \).

Similarly, the impedance at any of the nodes, looking from the right, is also \( R \) (consider first the inner most box \( B_n \) on the left and move gradually out). At node \( N_1 \) therefore, one sees impedance of \( 2R \) on either side (R+R).

The current \( I \) consequently splits equally between the right and left branches. The current in the right branch again splits equally at node \( N_{i-1} \) between the lower and the right branches (resistances \( 2R \) and \( R+R \)). In fact, a similar equal splitting takes place at each node on the right. There are such nodes to the right where this splitting takes place. The current flowing through the right most \( 2R \) into the operational amplifier is therefore \( I.2^{-1} \) if the bit \( i \) is one and zero otherwise i.e. it is \( I.a_i.2^{-1} \) where \( a_i \) is the value of bit \( i \).

If several bits are \( 1 \), the corresponding switches would each give an output of \( V_R \). By the principle of superposition, the current fed into the operational amplifier is the sum of the individual contributions due to each of these inputs occurring in isolation i.e.

\[
\sum \{I.a_i.2^{-1}\}
\]

We can see that \( I = V/3R \), since switch \( i \) sees an impedance \( 2R + (R + R)/(R + R) \), i.e. \( 3R \).

Since this current has all to flow through the gain resistor \( 3R \), the voltage at the output of the amplifier will be

\[
I.3R.a_i.2^{-1} \quad \text{or} \quad V_R^* a_i.2^{-1}.
\]

In contrast with the wide range of resistor values used in the weighted resistor D/A Converter, only two values of resistors (\( R \) and \( 2R \)) are used here. Because of the proximity of the values of the two resistors, it is easier to find resistors with similar temperature:
coefficients and exactly matched values. As shown in the analysis, only the ratio of the two resistor values is important and not their absolute values: with increase or decrease of temperature, the values of the resistors R and 2R might change, but the ratio between the two would remain constant. The output therefore would be independent of temperature.

**Inverted Ladder DA Converter:**

Weighted resistor D/A Converters and D/A Converters with resistor ladders have a resistor network between the analog switches and the operational amplifier (Fig. 2.5). These work well for all practical purposes, but have the following disadvantages:

a) Any one bit of the digital input (when it is 'on') has to connect a voltage \( V_R \) to the Resistor Network point. There has to be a large voltage swing from 0 to \( V_R \) at the output of the switch.

b) Switching the voltage at the input of the resistor network from 0 to \( V_R \) changes the currents flowing through the resistors and causes appropriate voltage swings at various points in the network. The RC time constants of the parasitic reactances associated with the resistors limit the speed of operation. The resistor values should therefore be low for high speed operation.

c) For accurate operation of the switch however, the current drain on the switches should be low. This requires high resistor values. These two requirements are contradictory.

These problems can be solved by interchanging the resistor network and the analog switches (Fig. 2.6).

We saw that in a Resistor Ladder D/A Converter, the analog switch connects either a voltage \( V_R \) or ground to an appropriate point in the ladder network. This changes the current flowing through the ladder network. In the Inverted Ladder D/A Converter configuration (Fig. 2.6) on the other hand, the current through the resistors remains constant: the switches operate as current steering gates and channel the currents either to the summing point of the amplifier (which is at virtual ground) or to ground. Hence, the impedance of the ladder resistors can be high; parasitic reactances will have virtually no effect on the speed of operation.
2.2.3 Indirect D/A Converters

We have seen so far that D/A Converters convert the digital input into an analog signal directly, so these are called Direct D/A Converters. Indirect D/A Converters convert the digital input first into an intermediate parameter (e.g., pulse width or pulse frequency); this is subsequently converted into an analog voltage.

The advantage of this type of converters is that at the cost of conversion speed, less costly linear components can be used. These are therefore preferred for slow speed applications.

Fig. 2.7 shows the block diagram of an indirect D/A Converter.
Single Speed Pulse Width D/A Converter

For the pulse width type of D/A Converter, the counter functions as a timer. The number to be counted (N) is loaded into the counter as the starting count. A fixed frequency clock starts at time \( t = 0 \) and stops when the counter counts down to zero, i.e., after \( nT \) clock cycles (or time \( nT \) where \( T \) is the clock period). A timing pulse also starts at \( t = 0 \) and stops when the clock reaches zero (i.e., \( t = nT \)). This pulse is fed to an analog switch which connects the voltage \( V_R \) to the output as long as the input pulse is present. It thus converts this pulse into a constant amplitude pulse. This pulse is in turn fed to an analog integrator which converts it into a proportional voltage.

For a D/A Converter with a 12 bit counter and a clock frequency of 1 MHz the count down time from \( 2^{12} \) to 0 is 4 ms (i.e., \( T \times 2^{12} \)). For good integration accuracy, the LP filter should have a much higher time constant than the maximum expected pulse width of 4 ms. Assuming a ratio of 100 to 1, the time constant has to be 400 ms. This limits the speed of conversion.

Fig. 2.8 shows a typical single speed pulse-width D/A Converter. The LOAD signal loads the digital input into the counter and the 12 input NAND gate gives a "high" output as long as the counter is non-zero. This pulse controls the time for which the voltage \( V_R \) is integrated. Accuracy of this D/A Converter is dependent on the linear components - the analog switch, the resistors and the amplifier. By
choosing resistors properly (ratio between the sum of the input resistors and the feedback resistor to be low) fairly good accuracy can be achieved. Conversion speeds are low for this type of D/A Converters.

![Diagram of a 12-bit counter with parallel digital input, load, clock, disable, zero sense, SW, LP filter/integrator, amplifier, and analog output.]

**Fig. 2.8 Pulse Width D/A Converter**

**Dual Speed Pulse Width D/A Converter:**

The time taken for conversion in a pulse width D/A Converter depends on the word length (the number of bits) of the number to be counted, \(2^n T\) where \(n\) is the number of bits and \(T\) is the clock period. Conversion time will reduce substantially if the binary number is split into two bytes and each byte is converted separately (for a 12 bit D/A Converter, there is a factor of 64 reduction, from \(2^{12} T\) to \(2^6 T\)). The output of the composite converter is, clearly, the weighted sum of the outputs of the individual converters. Fig. 2.9 depicts a Dual Speed Pulse Width D/A Converter.

The six LS Bits are loaded into counter 1 and counted down to zero. This generates a pulse of width \(t_1\). Once counter 1 reaches zero, the clock to counter 2 is enabled and it is then counted down to zero. The less significant channel is scaled down by a factor of \(2^6\), as \(2^6\) is the weight factor between counters 2 and 1. The input resistors of LP filters 1 and 2 should be in the same ratio; e.g. 20 K ohms for LP filter 2 and 1.28 megohms for LP filter 1.
For a single speed pulse width D/A Converter, the time for counting down from 212 to 0 is 4 ms with a clock frequency of 1 MHz. For a double speed Pulse Width D/A Converter, the scale factor of 26 brings this figure down to 4 ms/64 = 64 us. This reduction places a stringent requirement on the accuracy of the time of integration. The analog switch is a source of error here because its response times for turn on and turn off are different. For a 0.05% error, difference between turn-on and turn-off must be less than 64 us x 5 x 10^-4 = 32 ns. This is very difficult to attain for any analog switch.

To take care of this, the clock frequency may be lowered by a factor of 4 to 250 kHz. The maximum pulse width then becomes 256 us. The difference between turn-on and turn-off times then can be as high as 128 ns or 0.05% of 256 us. Analog switches satisfying this conditions are available.
Pulse Frequency D/A Converter

In the pulse frequency type or pulse rate of D/A Converter, the number to be converted (n) is loaded into a register which controls the clock frequency to be proportional to N (this is done by using a "binary rate multiplier" whose operation is too involved to describe here). The clock pulse frequency is therefore proportional to N. This clock pulse sequence is fed to an analog switch which, as above, ensures that the amplitude is constant. This pulse sequence is again fed to an integrator which converts it into a proportionate voltage.

The Pulse Rate D/A Converter of Fig. 2.10 consists of a Binary Rate Multiplier which has the parallel digital data as input. The BRM gives out a train of pulses, the frequency of the pulses being proportional to the digital input.

![Diagram](image)

**Fig. 2.10 Pulse Rate D/A Converter**

The analog switch S needs to be fast as it has to accept and transmit a large number of pulses within one conversion time whereas for the Pulse Width D/A Converter, the switch receives and sends out only one variable width pulse. It is very difficult to realise fast
analog switches which maintain a very high overall precision with respect to pulse width. Hence Pulse Rate D/A Converters are normally used only for slow operation. Typically, assuming a 20 ns pulse width error, one needs a pulse width of at least 80 ns to maintain a switch accuracy of 0.025%. For a 12 bit converter, this means a conversion time of 320 ms.

2.2.4 Bipolar D/A Converters

A unipolar D/A Converter can convert only unsigned numbers. The D/A Converters described so far fall in this category. For conversion of positive as well as negative numbers, one needs Bipolar D/A Converters. These require both positive and negative reference voltages; the reference voltage of proper polarity is selected depending on the sign of the input word.

![Bipolar D/A Converter Diagram]

Fig. 2.11 Bipolar D/A Converter

This requires that the switch which selects the reference supply should have very low impedance since it has to switch the current
supplied to the entire ladder network. Conversion of negative numbers is simpler in the offset binary mode. Here, a constant offset current is provided at the input of the operational amplifier. This offset current is adjusted to be equal to the current of the MSB which, in this case, is the sign bit.

2.2.5 Multiplying D/A Converter

A multiplying D/A Converter (MDAC) accepts two inputs - a digital word and an analog voltage. Its output is the product of these two. A parallel D/A Converter can be considered to be a special case of a multiplying D/A Converter, where the reference voltage is fixed.

In a one quadrant multiplying D/A Converter, both the reference voltage and the digital input take only positive values. Two quadrant MDCA's Converters are of two types:

a) a bipolar D/A Converter which permits the digital input to be bipolar while the analog reference remains unipolar and

b) a unipolar D/A Converter which accepts a bipolar analog signal and a unipolar digital word.

A four quadrant MDAC is one where the analog signal and the digital word are both bipolar. D/A Converter 2701 is an example of a four quadrant MDAC from ILC Data Device Corporation, U.S.A. It accepts either a positive or a negative reference analog voltage; the digital input may also be positive or negative. It has a 12 bit input register, a 12 bit holding register, a 12 bit multiplying CMOS D/A Converter and a current to voltage converter operational amplifier. The input and holding registers can be configured for single buffered, double buffered or direct flow-through operation.

2.2.6 Specifications of D/A Converters

The technical specifications of a device or system enable an intending user to determine whether or not it will be satisfactory for the application he visualises. The following are the more important technical specifications of a D/A Converter.

(1) Input Specifications: The D/A Converter accepts two inputs: the digital number to be converted and the analog reference voltage. The digital input can be fed either serially or in parallel, and can use any convenient coding scheme (see Sec.
2.4) one's complement or two's complement binary, offset binary, or sign magnitude binary (even non-binary codes are in principle possible but not common for D/A Converters). The current drawn by each input terminal is a relevant specification and is expressed in terms of equivalent TTL or CMOS loads. The specification "loading: n" means that the input draws the same current as "n" standard TTL (or CMOS) circuits. The current drawn from the reference supply has also to be specified.

(2) Output Specifications: The converted analog signal is the only output of the D/A Converter. The important specifications are its range (usually 0 to 5 volts) the DC output impedance and the maximum current that can be drawn (typical values: 0.05 ohms and 10 mA). The DC supply voltage(s) required and the current(s) drawn by the unit are also necessary, though not critical, specifications.

(3) Resolution: The length of the input word (usually 8, 10, 12, or 16 bits) determines the least count or resolution of the system: the minimum separation possible between two adjacent inputs or outputs. The resolution of a 10 bit A/D Converter with a range of 5 volts is \(5 \times 2^{-10}\) volts.

(4) Offset Error: Offset Error is the extent to which the transfer function of a D/A converter deviates from the ideal.

(5) Linearity Error: Let us consider digital inputs \(D_1\) and \(D_2\) (say 111000 and 000001) in which different sets of bits have the value 1. Let the corresponding analog outputs be \(A_1\) and \(A_2\). What happens for input \(D_3\) (111011) for which both these sets of bits have the value 1? Ideally, if the system is linear, the corresponding output \(A_3\) should be \(A_1 + A_2\), by the principle of superposition. In practice, however, this is not necessarily the case. The difference between these two quantities \(A_3\) and \(A_1 + A_2\) is the 'linearity' or 'summation' error. Typically, linearity error can be 0.01% to 0.05% of full scale range.

(6) Setting Time to Percentage Accuracy: For a change in digital input extending over the full scale, the time required for the D/A Converter output to settle to within the desired accuracy is defined as the settling time. Setting times (for ± 0.05% accuracy) are usually in the range of 5 to 20 microseconds.

(7) Temperature Coefficient: The temperature coefficient of gain and offset are defined in terms of the 'average' deviation
over a range of temperature variation (typically 20 ppm/°C).

DAC-8528 is a typical D/A Converter made by ILC Data Device Corporation, U.S.A. and has the following specifications:

(a) Parallel digital input with offset binary coding TTL compatible input.
(b) Output voltage ranges: ±2.5, ±10, 0 to -5, 0 to -10 volts.
(c) Maximum output current: 10 mA
(d) DC Output Impedance: 0.05 ohms.
(e) Resolution: 12 bits.
(f) Linearity Error: ±0.025% of full scale range (maximum).
(g) Settling Time to: ±1 LSB 50 ns max.
(h) Temperature Coefficient: Gain 30 ppm/°C, Offset ±15 ppm/°C.

2.3 ANALOG TO DIGITAL CONVERTERS

The process of analog to digital (A/D) conversion is similar to that of weighing an object using a regular balance. We place the given object (of unknown weight) in one pan of the balance (say on the left hand side) and a trial weight \( W_L \) which is the sum of standard weights \( (W_1, W_2 \text{ etc.}) \) on the right hand side (see Fig 2.12). If the balance tilts to the left, indicating \( W_L \) is too small, we increase \( W_L \) by adding weights on the right hand side; if it tilts to the right, \( W_L \) is too large and we decrease the weights. After a few trials, we achieve the best balance. The weight of the object is taken to be the sum of all the weights on the right hand side. The error in the weighing process will be less than or equal to the smallest standard weight \( (W_B) \) available to us, provided that the sensitivity of the balance does not pose a limitation.

For analog to digital conversion also, we compare the unknown voltage \( V_X \) against a trial voltage \( V \) which is the analog equivalent of a trial binary fraction \( D_T \)

\[
V_T = V_R D_T
\]

where \( V_R \) is the reference voltage fed to the D/A Converter. If \( V_T \) is too small, \( D_T \) is increased and vice versa. The conversion process is complete when the best match is achieved. The digital equivalent of the input voltage \( V_X \) is the fraction \( D_T \) giving this best match. The error in conversion will be less than or equal to the smallest increment possible, i.e. the magnitude corresponding to the least significant bit.

Thus,
\[ V_x = V_R \sum_{i=1}^{n} a_i 2^{1-i} = V_R (a_1 2^{-1} + a_2 2^{-2} + \ldots + a_n 2^{-n}) \]

where \( a_i \) are the values of the individual bit stages and the maximum error is \( V_R 2^{-n} \), the weightage attached to the least significant bit.

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**Fig. 2.12 Weighing Compared with A/D Converter**

A/D Converters adopt this broad principle of operation to varying degrees of detail. Some differ primarily in the strategy adopted to vary \( D_L \) and \( V_L \) for achieving the best balance.
2.3.1 Basic Concepts in A/D Conversion

Transfer Function:

An A/D Converter accepts a given analog voltage $V_X$ and an analog reference voltage $V_R$ as inputs. It gives a digital fraction $D$ as output. Fig. 2.13 represents a block diagram and transfer function of a typical A/D Converter.

The digital output $D$ is expressed as a proper fraction. The decimal point is taken to be at the extreme left of the sequence.

For a binary number of radix $2$,

$$D = a_1 2^{-1} + a_2 2^{-2} + ... + a_n 2^{-n} \quad ...(1)$$

where coefficients $a_1, a_2, ..., a_n$ can take the values zero or one.

$$D = \frac{V_X}{V_R} \quad ...(2)$$

defines the Transfer Function (Fig. 2.14), for the A/D Converter. It can be expressed as

$$V_X = V_R(a_1 2^{-1} + a_2 2^{-2} + ... + a_n 2^{-n}) \quad ...(3)$$

![Fig. 2.13: Block Diagram of an A/D Converter](image-url)
Quantization Error:

For an input varying continuously over the entire permitted range and taking an infinite number of values, the output can attain only a finite number of values \(2^n\) values for \(n\) bits). The converter thus has a least count (difference between two adjacent values of output) of \(V_R \cdot 2^{-n}\). This implies that there can be an error in conversion. This error is defined as 'Quantization Error' (see Fig. 2.14).

![Transfer Function and Quantisation Error](image)

**Fig. 2.14 Transfer Function of an A/D Converter and Quantisation Error**

For example, let us consider a 4 bit A/D Converter. The weightage of the least significant bit is \(\frac{1}{16}\) and that of the next bit is \(\frac{1}{8}\). Let us consider an input corresponding to \(\frac{5}{8}\). The output in this case can be \(\frac{3}{4}\) and there is no error. On the other hand, for an input corresponding to \(\frac{6}{8}\) there is no output which is an exact equivalent. The nearest possible output value is \(\frac{3}{4}\). However, in most A/D Converters, there is no guarantee that the output will be the nearest possible value. Depending on the direction from which the value is approached, the output may be either of the two adjacent values nearest to the exact value - lower or higher: \(\frac{7}{8}\) or \(\frac{9}{8}\) in this case. The quantization error will therefore be either
\[
\begin{vmatrix}
3 & -9 \\
16 & 64
\end{vmatrix}
\text{ i.e. } \frac{3}{64} 
\text{ or } 
\begin{vmatrix}
1 & -9 \\
8 & 64
\end{vmatrix}
\text{ i.e. } \frac{1}{64}
\]

2.3.2 Direct A/D Converters

Basics of Parallel Feedback Servo A/D Converters

Parallel feedback servo A/D Converters use the general strategy for conversion that we described in section 2.3. Here the value of the trial number (the digital fraction \( D_T = \sum \frac{a_i}{2^i} \)) is increased or decreased in steps of \( 2^{-1} \) depending on whether the trial voltage \( V_T \) is less than or greater than the input voltage \( V_X \). Fig. 2.15 shows a schematic diagram of the converter.

![Parallel Feedback Servo A/D Converter Diagram](image)

**Fig. 2.15 Parallel Feedback Servo A/D Converter**

The summing amplifier compares the input voltage \( V_X \) and the trial voltage \( V_T \) (which is the output of the D/A Converter). The output of this amplifier is used to control the direction in which the up/down converter proceeds (up if \( V_T < V_X \) and down if \( V_T > V_X \)). When \( V_X = V_T \) (i.e. when \( |V_X - V_T| < V_{Ref} \cdot 2^{-1} \)) the counter stops, because this is
the best match possible. This function is achieved by the threshold logic associated with the summing amplifier. This method, it will be noticed, is very similar to weighing in a balance,

(a) starting with an arbitrary trial weight,
(b) determining, from the way the balance tilts, whether the weight is too high or too low and
(c) decreasing or increasing it monotonically, one unit at a time, till balance is achieved.

It is also very similar to that of a servo control system. A control signal (Vc) is fed as input to the system. This is compared with the value of the output signal (Vp) which is to be controlled. The error signal (the difference between the two) is amplified and used to correct or vary the controlled signal in the desired direction so as to minimise the error. This type of converter is therefore called a parallel-feedback servo-converter; note the parallel connection between the up-down counter and the D/A Converter in the feedback path.

This type of feedback works in both directions; hence, the counter can start at any arbitrary value and count up or down as required, to achieve a match. Consequently, there is no need to reset the counter after each conversion.

Since the counter moves up or down only one step per clock cycle, the number of clock cycles required for conversion to be complete can vary depending on how good a match the first trial value is. In the worst case, i.e., if the first trial value is zero and the input corresponds to full scale or vice versa, the difference is 2^n and conversion would require 2^n steps, where n is the number of bits.

Adjusting the threshold for comparison is important. Since the counter stops if \(|V_c - V_x|\) is less than the threshold, this defines the accuracy of conversion. Hence, the threshold should not be higher than the least count. If it is much smaller than the least count, the counter may never stop; even the two best possible output values could result in error signals and the system would remain hunting between these two values.

As the counter is not reset to zero between successive conversions, it simply moves up or down from its previous value to the next value, driven by the comparison error signal. This is most convenient if the counter has to repeatedly digitize a single changing signal. Since the variation between successive conversions will, in general, be small, the time required for conversion will also be small.

If the A/D Converter has to be switched between channels, i.e. it
is connected through a multiplier, there may be large variations between successive inputs. Conversion times can be quite high in such cases. Typical worst case conversion times for such converters are in the range of a few milliseconds (1 microsecond clock cycle and 12 bits for the digital output yields $2^{12}$ us or 4.096 ms).

**Successive Approximation A/D Converter**

We have earlier compared the process of A/D conversion to that of weighing, using a pair of scales and fixed weights. In the case of the successive approximation A/D Converter, the process of conversion is similar to that of achieving balance, trying first the largest weight available and successively going downwards. For instance, let us say that the object to be weighed is 603 gms in weight and we have standard weights of 800, 400, 200, 100 and 50 gms. First we try 800 gms (step 1) and find it too large. So, we discard it and try 400 (step 2). This is too small. So we add 200 (step 3) and this still is too small. We then add 100 (step 4) and find it too large, so we remove 100 and add 50 (step 5). This is too large. Since we can't go any further, we step and conclude that the weight is between 600 and 650 gms. The general procedure is that, in the $i^{th}$ step, we try changing the weight by $A_i 2^{-i}$ (in this case, 1000 x $2^{-1}$ gms). We merely add this weight if the weight tried previously was too small. If the previous weight was too large, we reduce this (by removing the weight added in the previous step, i.e. $A_i 2^{i+1}$ and adding $A_i 2^i$).

This exact method is used in the successive approximation A/D Converters (Fig. 2.16). The shift register contains the trial value being compared with the input signal (finally, it will contain the digital output obtained as a result of the conversion). The D/A Converter converts this trial value into an analog voltage $V_t$ and compares it with the input signal $V_i$. The output of the comparator ($V_t - V_i$) indicates whether the value tried out was too high or too low and functions as the control signal ($V_i$) which determines whether a higher or a lower value is to be tried during the next step.

Let us now examine its operation. Let us assume the analog reference voltage is $V_R$. The range of the A/D Converter will also be $V_R$, since the maximum output of the D/A Converter (for all input bits being 1) will be $V_R$.

First step: $V_i$ is compared against $+V_t$ which, in this step, is $V_R/2$ (or $V_R 2^{-1}$). The MSB of the shift register is 1 and all other lower bits are zero.
Second step: If $V_t < V_R$, during the first step, i.e. $V_C$ is positive, a higher $V_t$ has to be tried. The second bit of the shift register is made 1 and $V_i$ is compared against $V_R(2^{-1} + 2^{-2})$.

If $V_t > V_R$, i.e. $V_C$ is negative, a lower $V_t$ has to be tried. The first bit of the shift register is made zero and the second bit one. $V_i$ is compared against $V_R(2^{-2})$.

Subsequent Steps: In general, during the $i^{th}$ step, if $V_t < V_R$, $V_C$ is positive and a higher $V_t$ has to be tried; hence the $i$th bit of the shift register is made 1.

If $V_t > V_R$, $V_C$ is negative, and a lower $V_t$ has to be tried; hence the $(i-1)^{th}$ bit is made zero and the $i$th bit is made 1.

The process terminates after $n$ steps, where $n$ is the number of bits in the shift register. The maximum error during step $i$ will be $V_R, 2^{-i}$. The trial voltage approaches the input voltage $V$ in a series of successive approximations; hence the name of this type of
converter. The final error or least count of the converter is $V_i 2^{-n}$ where $n$ is the number of bits in the shift register.

The main advantage of this method is that it is simple and fast. The time required for conversion is fixed, irrespective of the value of the input. Exactly $n$ clock cycles are required for achieving a conversion accuracy of $n$ bits. As against this, the parallel feedback servo-converter may take anything up to $2^n$ clock cycles per conversion.

A number of operations have, however, to take place in a single clock cycle:

(a) the shift register is set,
(b) the D/A Converter settles down and
(c) the amplifier responds to the new inputs.

Since the voltage swings in a single clock cycle can be as much as half of full scale, timing is critical. The most time consuming operation is the settling down of the comparison amplifier.

There is a trade off between accuracy and speed of conversion (the larger the accuracy desired, the greater the number of clock cycles required - one clock cycle per bit). This, however, is much less severe than in the case of the parallel feedback servo-converter where each additional bit of accuracy doubles the number of clock cycles required.

Where speed is not a critical requirement, the limit to accuracy is set by the accuracy of the D/A Converter and the comparator. At high speeds of operation, the transient behaviour of the various units becomes very important. Switching transitions in the digital switches and RC delays in the ladder network as well as response time of the comparison amplifier might cause glitches in the D/A Converter output.

Typically, successive approximation converters can provide up to 12 bit outputs. Accuracy is in the range of 0.05% and conversion speeds in the range of 100 us per conversion, or 10,000 conversions per second. At such speeds, one has to use high speed operational amplifiers with low offset voltages as comparators.

2.3.3 Indirect A/D Converters

An A/D Converter is called indirect if the input analog signal is first converted into another intermediate signal which is subsequently used for providing a digital output. In general, the input signal is converted into a proportional parameter (usually the width or repetition frequency of a pulse). Converting this into a proportional number is straightforward and can be accomplished by means of a
counter or a clock-counter combination.

Simple Ramp Comparison A/D Converter

Figure 2.17 shows the circuit diagram of a simple ramp comparison A/D converter. Here, the input signal $V_x$ is compared with a saw tooth or ramp signal $V_s$. If the saw tooth starts at time $t = 0$, $V_s = t V_R$. A clock of frequency $f_C$ and the converter which counts the clock pulses, also start at $t = 0$. Let us assume that the comparator gives an equality signal at time $t_x$, when $V_s = V_x$. Then, $t_x$, one can see, will be $(V_x/V_R)$. The number of clock pulses emitted till then (and therefore the contents of the converter) will be $(V_x/V_R) f_C$. This number will be gated into the register and given out as the digital output. The cycle is completed when the counter reaches the maximum count. The overflow signal from the counter is used to reset the counter and the ramp generator; the next cycle can start thereafter.

![Diagram of Simple Ramp Comparison A/D Converter](image_url)

Fig. 2.17 Simple Ramp Comparison A/D Converter
In a simple ramp comparison converter (Fig. 2.17), the ramp is generated using analog techniques. The accuracy of conversion in this case would depend on the linearity of the ramp generator and the accuracy of comparison. Typical values of parameters are: clock frequency 10 MHz; comparison accuracy ± 1 mV; conversion accuracy 0.005% of full scale; conversion time: 0.4 ms (12 bits).

A difficulty with this type of converter is that it cannot be adapted for operation with negative inputs, because the ramp cannot be bipolar. While the circuit is simple and inexpensive, it suffers from the disadvantage that conversion accuracy critically depends on the linearity of the ramp generator and its time constant.

**Precision Ramp Comparison A/D Converter:**

Precision ramp comparison converters use a much more accurate saw tooth signal generated, say, by connecting a D/A Converter to the counter (Fig. 2.18). While this increases complexity, it has the advantage of high accuracy and stability. Another advantage is that the converter lends itself to easy adaptation for multichannel operation. The counter and D/A Converter can be common, while there
Data Conversion Principles

can be a separate comparator, gate and data register for each channel. When comparator C indicates equality, gate G operates and gates the counter contents into register R which contains the digital equivalent of the input signal \( V_{X1} \).

It can be seen that the single channel precision ramp converter is very similar to the parallel feedback servo-converter; if its counter is reset to zero after every conversion, it would always count up, as in the precision ramp converter.

While the precision ramp converter is much more accurate than the simple ramp converter, it is also much more complex and therefore more expensive.

Up-down Integration A/D Converter

In an up-down integration converter, a dual slope method is used to make operation insensitive to time constant variations. The input voltage \( V_X \) (Fig. 2.19) is integrated for a fixed period of time \( T_X \) starting with a low voltage (say zero). The output of the integrator therefore rises linearly to the level \( \frac{V_X \cdot T_X}{T_C} \) where \( T_C \) is the time constant of the saw tooth (the time taken for the ramp voltage to equal the voltage being integrated). After this, a fixed reference voltage \( -V_R \) (of opposite polarity) is used as the input to the integrator. The time \( T_X \) taken for the output to go from the value

\[
\frac{V_X}{T_C} \cdot T_X \text{ to zero is given by } \left[ \frac{V_X}{T_C} \cdot T_X \cdot \frac{T_C}{V_R} \right] \text{ or } \frac{V_X}{V_R} \cdot T_X
\]

This time would increase for smaller values of \( V_X \) and decrease if \( V_R \) were to be increased. It would be \( T_X \) if \( V_R = V_X \).

This time \( T_X \) (which is proportional to \( V_X \) and depends only on \( T_X \) and \( V_R \)) is the intermediate analog parameter used. This can be digitised using a clock counter mechanism. The counter contents can be gated out into a register. The main advantage of this type of converter is that the result is independent of the time constant of the ramp. This time constant cancels out because of the dual slope method. It is also less sensitive to noise because the input signal is integrated over a reasonably long period of time.

The voltage on the ramp generator is zero at the beginning of the conversion and at the end as well. The comparator output itself is used to signal both the start and the completion of the conversion cycle. Comparator offset will therefore not introduce errors, as it
would effect both the start and the end equally.

\[
T_X = \frac{V_R}{V_X} \cdot T_P
\]

Fig. 2.19 Principle of Operation of a Dual Slope A/D Converter

This type of converter can be adapted for multichannel operation quite easily. The input of the converter can be switched between the
channels after each conversion cycle. There can be separate output
data registers for each channel.

2.3.4 Specifications of Analog to Digital Converters

An A/D Converter is a rather complex piece of equipment; differences
between converters can occur along several dimensions: the technology
used (discrete, keyboard or I/C), the types of components used, the
technique used for conversion, the input and output specifications and
functional characteristics. We shall briefly consider below the
technical specifications of A/D Converters.

**Input:** As in any analog device, the main specifications on input
are the Input Range (the maximum permissible magnitude of the input
voltage signal) and the input impedance. The input range is typically
0 to 10 volts and the input impedance, usually 50 ohms.

**Output:** The output is made available as a digital number and can
therefore be expressed in one of several codes: sign and magnitude,
two’s complement, one’s complement or offset binary modes. Loading
permitted on each output bit stage is expressed in terms of the number
of standard TTL or CMOS input loads that can be driven from each
output terminal.

**Power supplies:** Since the system contains both digital and analog
circuits, the appropriate power supplies have to be used. The
characteristics of the analog power supply will have to be carefully
specified because the performance of the converter will naturally
depend on these. Supplies for the digital and analog systems should
be adequately isolated from each other.

**Resolution:** The resolution or least count of the A/D Converter is
the minimum difference required between two inputs for them to be
resolved as being different. Obviously, this determines the number
of bits in the output word (resolution = V_{R} \times 2^{-n}).

**Linearity:** Ideally, an A/D Converter yields a digital output
which bears a linear relationship with the analog input. In practice,
there may be deviations. Accuracy and linearity errors are measures of
such deviations and can be expressed either as parts per million of
the full scale range, or as a fraction of the least significant bit.
The analog voltage required to just turn on each bit of the converter
can be separately measured. In an ideal converter, the voltage
Data Conversion Principles

required to turn on any combination of bits will be equal to the sum of voltages required to turn each of these bits on singly. The difference between these two quantities is the linearity error. Typical values are in the range of 0.2% of the full scale. The effective error is the cumulative effect of zero error, gain error non-linearity error and noise.

Conversion Time: The total time required to complete one conversion or measurement is called the conversion time. Typical values are in the range of 1 to 25 µs per conversion, depending on circuit speeds and the number of bits.

Aperture Time: The time for which the input voltage has to be held invariant for a conversion to be performed is the aperture time. Where there is no provision for the input to be quickly sampled and "held", the signal has to remain invariant till conversion is complete; aperture time will therefore be the same as the conversion time. Where a sample and hold circuit is used, the aperture time can be much less (of the order of 50 ns).

Temperature Coefficient: The values of parameters of components used in the converter can vary with temperature causing conversion errors. These errors are expressed as parts per million or percentage fractions of 1 LSB. They are computed by observing the error caused when the equipment is taken from room temperature to the maximum or minimum permitted operating temperature. Typical values are in the range of 20 ppm/°C.

2.4 REPRESENTATION OF SIGNED NUMBERS

We have seen how scalars can be represented as numbers in the decimal and binary systems. In the decimal system, there is only one standard convention for representing signed numbers. There are, however, several alternative methods for doing this in the binary systems. Most of these codes represent positive numbers the same way and differ only in the way they represent negative numbers.

Sign-magnitude Method of Representation:

The most straightforward manner of representing a number is in the sign and magnitude form. This is the standard way numbers are represented in the decimal system; a negative number with magnitude 5
is represented, for instance, as -5. Similarly in the binary system, the fraction -5/8 is represented as 1101; the most significant bit is used to represent the sign (0 for positive and 1 for negative numbers) and the remaining bits represent the magnitude. Here, 0000 and 10000 both represent zero.

The advantages of this system are that it is simple and most convenient to use in D/A Converters where it is necessary to provide for smooth and linear transitions from small positive voltages to small negative voltages. For example, the transitions from 10001 to 00000 and from 00000 to 00001 will be symmetric even if the D/A Converter is not an ideal one. Arithmetic, however, becomes complicated; if two numbers with opposite signs have to be added, one of them has to be complemented e.g. to compute 1/4 + (-1/8) (i.e. 0010 + 1001), the negative number has to be 2's complemented and added (010 + 111 = 001) to give the correct result. Also, since there are two different codes for zero, interpretation by hardware becomes complicated.

One's Complement representation

In this code, positive numbers are represented in the sign and magnitude form while negative numbers are represented by the 1's complement (obtained by substituting 0 for 1 and 1 for 0) of their magnitude. For instance, -1/8 is represented as 1110 (the first bit represents the sign, and the three remaining bits are the 1's complement of 001 or 1/8).

Where addition or subtraction yields a carry in the MSB, it is necessary to add it to the least significant bit (end-around carry). Let us, for instance, compute 1/4 + (-1/8) (i.e. 0010 + 1110). The result (0000) would be wrong unless the end around-carry is considered and added, making it 0001.

Calculating the magnitude of negative numbers is easy because it merely involves bit-wise complementation but arithmetic becomes more involved. Using one's complement representation for D/A conversion also creates difficulties because, when the number is negative, a 1 has to be added to the LSB for correct results.

Two's Complement Representation

Positive numbers are represented in sign magnitude representation while negative numbers are represented in the two's complement mode (obtain one's complement and add 1 to the LSB; e.g. the two's
complement representation of \(-1/8\) is \(1\lll\).

Computation is simple in this system because there is no conversion involved in subtraction or addition of two numbers with different sign (e.g., addition of \(1/4\) and \(-1/8\) can be performed by adding \(0010\) and \(1\lll\). This yields \(0001\) or \(1/8\) which is the required answer). It has the same code for positive and negative zero, except for the sign bit. A disadvantage of the two's complement representation is that arriving at a representation for a negative number involves addition (of \(1\) in the LSB). A further problem is that all the bit stages change their value for a shift from zero to negative values (e.g., \(0\) is \(0000\) while \(-1/8\) is \(1\lll\)). In practice, this can cause glitches, discontinuities and non-linearities near zero, during D/A conversion. Using two's complement representation for D/A conversion has the disadvantage that a \(1\) has to be added to the LSB when the number is negative.

Offset Binary Code

The offset binary code can be visualised as a code in which a fixed offset (of \(+1\)) is applied to all numbers, so that the maximum negative number in the range is represented by zero. All other numbers are similarly offset. The offset binary code representation is very close to the two's complement representation and can be obtained by merely complementing the sign bit of the two's complement representation (e.g., \(-1/8\) is represented as \(0\lll\)).

The advantages are that it has only one code for zero and that it can be easily converted to the 2's complement code which is convenient for computations. Like the two's complement code, it too has the disadvantage that there is a discontinuity near zero.

Fig. 2.20 shows how numbers in one representation can be converted into any other representation. Since some codes are closer to each other than to others, conversion between them is straightforward. It is therefore simpler in some cases to effect a code conversion from one code to another (e.g., from sign magnitude to two's complement) by going through an intermediate code (one's complement).

Gray Code

All the codes that we considered so far have the property that the bit positions have different weightages. A consequence of this is that a transition between two adjacent numbers in the code often involves a
change of more than one bit (e.g. the transition between 3/8 and 1/2, i.e. 0011 and 0100 involves a change in two bits).

Fig. 2.20 Convention Between Codes

This can create problems in shaft encoders which are used to convert an angle into an equivalent digital number. Let us consider for example, the output having to change from 0011 to 0100 as the shaft rotates. If the encoder is not properly aligned, all the bits may not change simultaneously; the output would assume spurious values during the transition, say thus: 0011 to 0111 to 0101 to 0100). This problem (which is similar to that of glitches in A/D Converters) is very serious, but cannot occur if each unit step up or down involves a change in only a single bit. This is achieved in Gray codes. However, the bit stages in Gray codes do not have associated weightages; hence, D/A conversion of numbers represented in gray code.

Conversion between Gray code and binary code can be done using the following relationships, where $B_i$ and $G_i$ are the $i^{th}$ bits in the binary and Gray code representation respectively.
To convert from binary to Gray code:

\[ G_0 = B_0 \]
\[ G_i = B_{i-1} \oplus B_i \quad \text{i.e.} \ 1 \text{ if } B_i \neq B_{i-1} \]
\[ \emptyset \text{ if } B_i = B_{i-1} \]

To convert from Gray to binary code:

\[ B_0 = G_0 \]
\[ B_i = B_{i-1} \oplus G_i \quad \text{i.e.} \ B_{i-1} \text{ if } G_i \text{ is } \emptyset \]
\[ B_{i-1} \text{ complemented if } G_i \text{ is } 1. \]

2.5 SPECIAL CIRCUITS

We said earlier that measurement and control can be accomplished using digital systems if the parameters measured can be converted into a form suitable for digital representation. This requires that the outputs of instruments and sensors be connected to an A/D Converter. This is possible only if the input specifications of the A/D Converter are compatible with the characteristics of the output signal which is to be connected to it. Where such compatibility does not exist, it becomes necessary to use special circuits in between to achieve it. For example, where the common mode voltage levels are not compatible, isolation amplifiers are required. Instrumentation amplifiers are used if the signal amplitude is too low. Where the signal varies significantly within the time taken for A/D conversion, the output could be erroneous. In such situations, a sample and hold circuit is required; this would quickly sample the signal and hold the sampled value till conversion is complete. A multiplexer is required if a single A/D Converter has to be shared between several inputs. We shall study some of these circuits in the next section.

Isolation Amplifiers

Isolation amplifiers are required where a very high degree of isolation has to be provided between the signal source on the one hand
and the power supply and output circuitry on the other hand. They are used when there are high common mode voltage levels or extremely low common mode leakage currents are necessary. They are required, for instance, in biomedical sensing applications. EEG and ECG monitoring are examples where extreme isolation is necessary. Even more critical are monitoring of heart or brain signals during open-heart or brain surgery. Here, even extremely low voltage signals or leakage currents appearing through electrical probes might harm the patient.

Isolation amplifiers (Fig. 2.20) break the common mode signal path from the signal source. The amplified signal modulates an RF carrier signal. The modulated carrier is then fed to the output stage by transformer coupling. Even DC power is converted to AC and fed by transformer coupling to the input stage, where it is reconverted into DC.

The requisite degree of isolation between input and output stages can be ensured by suitably designing the signal and power transformers. A shield is also provided between the input and output stages to ensure isolation.

![Schematic Diagram of an Isolation Amplifier](image)

Instrumentation Amplifiers

Instrumentation amplifiers are useful when the output signal from an instrument or sensor is not adequate to drive the unit to which it has to be connected. Examples are transducers such as strain gauges and
thermocouples and biosensors such as those used for monitoring EEG, ECG and other body functions. These provide millivolt and microvolt signals, while A/D Converters require signal magnitudes of a few volts.

The main requirement of an instrumentation amplifier is precise and stable gain, since any variation in gain will appear like a variation in the output of the sensor. Gains of the order of 1000 are usually needed. The other requirements are very high input impedance, low output impedance, very low offset and amplifier noise and very high common mode rejection.

The schematic diagram of a typical instrumentation amplifier is shown in Fig. 2.22.

Operational amplifiers 1 and 2 constitute a differential input amplifier whose gain can be controlled by varying $R_1$. Amplifier 3 provides further gain. It will be noted that the loop $V_R$ to output has unity gain, so the output voltage is $V_R + G(V_A - V_R)$. Hence, $V_R$ can be connected to the reference voltage against which the output is to be measured or utilised.

![Fig. 2.22 Instrumentation Amplifier](image)

Sample and Hold Circuits

The main function of a sample and hold circuit is to "sample" a given (fast varying) signal at a specified instant and maintain or "hold" the input of, say, an A/D Converter constant at this level long enough for the conversion to be completed.

The unit has, as indicated by its name, two functions:

a) sampling or acquiring the value of the input (in this mode, the output of the unit follows the input and the circuit functions as a unity gain amplifier) and
b) holding or maintaining the sampled signal constant (in this mode, the output is maintained at a constant level, i.e. at the value of the input at time t when the transition from sample mode to hold mode occurs).

The sample and hold circuit (Fig. 2-23) consists of two stages of amplification. The first stage is operative only during the sample mode (the switch is closed) and causes the voltage on the capacitor to follow the input signal. The gain is usually unity. When the unit is switched to the hold mode, the charge on the capacitor is prevented from leaking; the voltage on the capacitor therefore remains at the level it was just before the switch to hold mode. The only path available for charge leakage is through the input impedance of the output amplifier. This determines the accuracy of the "hold" function.

The acquisition time is the delay between the start of the control pulse which switches the unit to the sample mode and the time the output reaches its proper value (equal to the input). This depends on the operation of the switch, the slewing time of the amplifier and the settling time for the output. It is usually in the range of a few usec.

![Schematic Diagram of a Sample and Hold Circuit](image)

**Fig. 2-23 Schematic Diagram of a Sample and Hold Circuit**

The aperture or delay time is the delay between the start of the control pulse which switches the unit to hold mode and the time the unit does this by opening the switch fully. To sample \( t - t_a \) where \( t \) is the aperture time. The aperture time is typically in the range of 100 n sec. Aperture or delay jitter is the range of variation of the aperture time. It reflects as a timing error on the instant of sampling. This jitter is usually a few nano seconds in magnitude.

The change in the output voltage during hold mode is defined as
droop. This is due to leakage of the charge on the capacitor. A small fraction of the input signal might appear at the output even during the "hold" mode. This is called feed through. This is caused by inadequate isolation provided by the switch in the open mode.

Multiplexers

A multiplexer is a many-to-one analog switch. It can, at any given time, selectively channel the signal appearing at any one of several inputs to the output. It is therefore useful where a single circuit or system has to be shared by (i.e., switched between) two or more channels. The inputs (Fig. 2.24) are all essentially connected to the common output through switches, one per input. At any given time, only one switch can be closed; all others must be open. An appropriate number of address selection lines (N where \(2^N\) is the number of multiplexer channels) are connected to a decoder whose outputs and used to specify which switch is to be energised and therefore which input is to be connected to the output.

![Block Diagram of a Multiplexer](image)

**Fig. 2.24 Block Diagram of a Multiplexer**

There should be good DC isolation between the switch drive and the analog signal path. Otherwise, the drive signal fed to the switch will leak through to the output. The switch should have very low leakage current and a very low on to off impedance ratio, so that the signal on the unselected channel is isolated from the output.
From the above considerations, electro-mechanical relays would seem to be the most convenient switches to use. These are, however, very slow. In addition, they suffer from the disadvantages of limited reliability, jitter and bulk. Electronic switches can assure transfer errors of the order of 0.01% and settling times of the order of a few microseconds. "On" resistance (for an 8 channel CMOS multiplexer) is about 300 ohms (maximum) and leakage current about 10 n nano Ampere. (maximum). Cross channel coupling is of the order of 80 db.