Inductance Characterization of Small Interconnects Using Test-Signal Method

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Abstract

The test signal method can be used to measure and model inductance parameters (self and mutual) of a very small interconnect especially in high-density IC's by using a test signal (of small known amplitude and frequency) and a D.C. signal along with a Differential circuit.

Other measurement techniques such as LCZ and TDR for measuring inductance parameters are faced with limitations of L values greater than 5nH. The Test Signal Injection compliments this method and facilitates measurement of very low L values, especially those encountered in high speed circuits. This technique is applicable in the designing and benchmarking stage and hence is used to model interconnect couplings before packaging and polysilicon layout.

An account of interconnect-substrate effects causing displacement currents that result in self-inductive effects is given. Small interconnects have been modeled as lumped elements of a transmission line to form a full system integrity analysis of the Test Signal Injection Method circuitry for circuit simulation using SPICE. A careful simulation procedure was carried out to determine the input parameters of test signal amplitude and frequency to accommodate the parasitics of the interconnect under characterization.

1. Introduction

Advances in VLSI Technology have resulted in more complex chips having millions of interconnections that integrate the components of a microprocessor, gate array, or high speed computer chip.

An electrical connection is characterized by three parameters: series resistance, capacitance and inductance. Series resistance can be important and is easily determined by the material and dimensions of the interconnect. Various characterization techniques such as: Four-Probe, Interference technique, Potentiometers and Van der Pauw structures [7].

Measurement techniques vary from destructive to non-destructive methods and from On-Chip to Off-Chip. Many characterization techniques exist for the extraction of parasitic capacitance (viz. Capacitance Based Characterization Method (CBCM) [1], on-chip measurement using Reference Capacitor [2], Quasi-Static Floating – Gate Capacitance Method [3], etc.

Some methods of inductance characterization are the LCZ and TDR techniques [4]. Parameter extraction using Multiple Reflections [5] is also used for long interconnects. Described below is a novel method to determine self and mutual couplings between short interconnects (including substrate effects) using a differential circuit.

2. Inductance Characterization

Among these package parasitics (RLC), it is believed that self inductance is the most critical factor in determining the simultaneous switching (also called delta –i or ground balance) noise on the chip power / ground buses, particularly for high speed CMOS application. LCZ technique is usually applicable at frequencies between 1 & 10MHz. The lower operating frequencies of the LCZ limits its measurements accuracy and therefore is considered most useful in characterizing interconnect structures with high L (> 5nH). This is considered a severe limitation in the characterization of MCM and high performance packages, both of which have a typically low L structure for high-speed signal propagation.

In addition, because the bandwidth of today's chips has reached hundreds of MHz or even GHz, the low frequency LCZ technique can be useful for characterizing structures with frequency independent parameters (L measured at 10 MHz can still be used at operating frequency of several MHz). Other improvised techniques include time domain based TDR technique and Test Signal Injection Method.

3. Inductance

The inductance is often defined as an integration of the magnetic flux linkage over a closed current loop with respect to unit current in the loop. It is known that the L of a section of a wire in the loop becomes meaningful only when the complete loop (hence the current return path) is defined. It is important to note, however, that such definitions is based on a quasi static assumption and is valid only when the total loop length is much smaller that the signal wave length (so that there is spatial variation along the path of the loop) [6].

At high enough frequencies, a ground plane in the proximity of the current loop will induce a mirror- image current at the opposite side of the ground plane flowing in an opposite direction according to the transmission line theory. Considering a section wire in the original loop, the wire and its induced return current in the ground plane actually forms a new "current loop" (the two ends of the wire are closed by the displacement current). Inductance of a high speed interconnect is therefore only related to the geometry of the interconnect and the proximity of its induced return current (Figure 1). Increasing the distance from the ground plane results in a higher L value and the lower C value for the same section of wire.

The new "current loop" between the substrate and interconnect produces a very weak magnetic field in a direction perpendicular to the loop area. The alternating test signal results in a changing magnetic field which in turn induces a small signal into the interconnecting wire. Each small element is responsible for the "extra induced current" which explains the self-inductance parameter. Thus, the current introduced and hence the resulting potential difference due to self-inductive impedance are directly related to the interconnect-substrate spacing and the dimensions of the interconnect.

4. Test Signal Injection Method

A test voltage signal V Sin(ωt), having a small but constant amplitude (1 mVp) and high frequency well above the system bandwidth is injected into the input of a unity gain power amplifier as shown (in figure 3). This signal is then fed into one of the coupled interconnects which lies close to the substrate.

The low magnitude alternating current generated in this short interconnect is responsible for producing a potential difference across a definite length of the interconnect.

Let us first consider an interconnect in an isolated environment (i.e. to say that the interconnect mutual L and C are ignored in the equivalent circuit assuming their effects to be only 2nd order. This is achieved by leaving all neighboring package interconnect leads open. This is compatible with the conventional inductance measurement using LCZ technique. But unlike the LCZ where we were limited to measurement of high L values, we have a situation where only self inductive parasitics of a single interconnect are involved. Considering the fact that we are dealing with high speed switching circuits, we now introduce the following lumped element package model.

In the lumped element package model, a package lead or an interconnect structure is modeled as a resistor, a capacitor and an inductor as shown in figure 2. The objective of constructing such a model is that it can be combined with other circuit models for a full system integrity analysis using SPICE. The lumped model is used to represent a package lead or interconnect. If one end of the package lead (point B) is shorted to the ground the circuit equivalent changes as in the adjoining figure. This is justified since the node capacitance is very small (of the order of femtofarads) and a continuous current is being pumped in from end A. As a result the capacitive node is charged immediately and the current enters the inter connect element to flow into $R_{L.}$ (Load resistance) and eventually to ground. This new impedance looking into it from point A is $Z_{eff} = R + Z_L Z_C/(Z_L + Z_C) = R + j\omega L\,(1 - \omega^2 LC)$

At a frequency much below the resonance frequency of the circuit (defined as $f_r = 1/(2\pi\,(LC)^{1/2})$), With ω of the order of a few MHz, L of a few nH and C of the order of a fraction of a femtofarad, $\omega^2 LC << 1$ and therefore Z_{eff} can be reduced to $Z_{eff} \sim R + j\omega L$. Thus at lower frequencies Z_{eff} is determined by Z_L (purely self-inductive component) and R. With increase in frequency signal wavelength shortens and the lumped model gradually becomes inadequate in modeling the package interconnect.

The potential difference produced by the current is next fed to a High-Pass Filter (to obtain voltage drop proportional to the high frequency component of the servo current).The output is then fed into one of the inputs of an Operational – Amplifier (differential circuitry) after passing through a Pre-Amplifier stage.

A d.c. signal equal to the r.m.s. value of the test-signal is fed into another Power-Amplifier(Unity gain) to produce current that is allowed to pass through a similar interconnect (similar resistivity and dimensions

This ensures that the resistive impedance of both the interconnects under consideration will be the same. The d.c. nature results in no transient parameters for this interconnect. Thus, the only similarity in the parameters of the two sets of interconnect wires is of their resistive impedance which is eliminated by the use of the differential circuit. What remains then is the potential difference across the first interconnect due to its self-inductance (resulting from the underlying substrate, as explained above). Thus, parasitics involved due to variables such as substrate material ,interconnect-substrate distance can be indirectly studied using self-inductance results.

The Op-Amp is shown in the figure with it's two inputs(one from the test signal interconnect and the other from the d.c. interconnect). The Op-Amp is made to work at a common bias voltage equal to the r.m.s. value of the test signal. This voltage when subtracted from the signal coming from the first interconnect gives the differential voltage due to self-inductance.

The above explained method was used to determine self-inductance. In situations where a large amount of circuitry exists (where mutual couplings are more prominent than self inductance substrate effects), we determine the total inductance using similar methods. However, this time around in order to model interconnects for determining parasitic coupling, we use frequency in the range of just a few MHz. Also, all neighboring package leads are closed to introduce coupling effects. Coupling inductances for interconnection separation of about a micron are 3-5 nH. Coupling capacitance values are in the range of a few femtofarads (about 3ff). In order to compensate for the increased coupling parasitics the value of the signal frequency is lowered by approximately one order, so as to maintain adherence to the lumped model. The differential output measured, here, is due to self inductance of the test signal interconnect and its mutual couplings with the surrounding circuitry. Having studied the individual self inductance parameters for an interconnect shunted away from other couplings (for a given substrate, linewidth and interconnect – substrate spacing), the mutual couplings can be determined as merely the difference between the total and self inductance values.

5. Simulation

The SPICE simulation model of the Test Signal Method is shown in figure 4. The lumped element model of the interconnects is highlighted by the dotted box. R_L Presents the load resistance connected to the interconnect. R_A R_B L_A and L_B are the respective resistance and inductance values of the probes that measure the drop across a definite length of the interconnect. R_C and L_C are the parameters of the final probes. In order to avoid probe parasitic interference we expect $R_A = R_B$ and $L_A = L_B$. Similarly, with the last set of probes.

A constant current source of (from the unity gain amplifier) feeds current to the interconnections. The entire setup is On-Chip and special care is needed in the layout of the probes so as to match their lengths and parasitics. The test circuitry is expected to lie very close to the interconnects under consideration so as to reduce the probe parasitics. This may be managed by using equal "coiled" probe lengths.

6. Conclusion

This simple schematic technique can be appropriately used for interconnect characterization. The SPICE Simulation model of this Injection method agrees well with the parasitic values encountered in VLSI chip interconnects and also suggests typical input signal parameters required for this characterization test.

Figure 1 : Original current loop and its induced image current due to proximity of ground plane

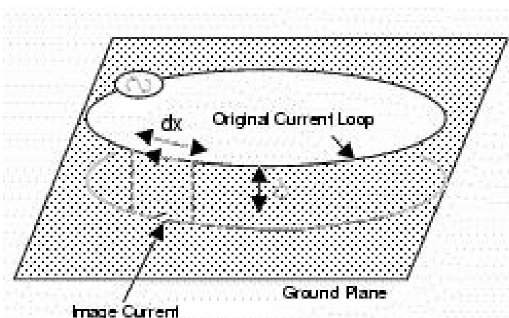
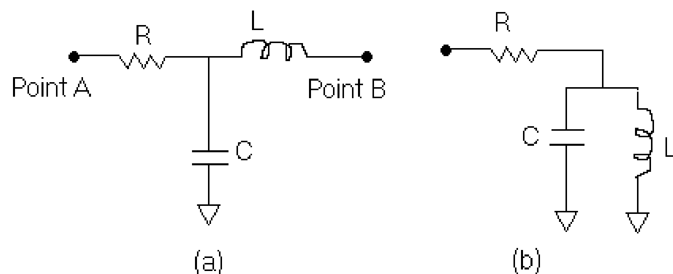


Figure 2 : Lumped-element equivalent circuit of an interconnect (a): model of a single package lead (b): model after one end of the lead is shorted to ground



Very few industry applicable techniques exist and a method to model parasitic values in the design stages is needed. The differential circuitry applied may provide the answer to this, as well as suggests means of studying and comparing parasitic transients for different resistivity substrate and interconnects. An optimization based on corresponding studies can lead to less substrate interference and less couplings among neighboring interconnects. Accuracy of measurements depends greatly on the assumption that the two interconnects have the same resistivity and dimensions. More so, even the Filtering circuit and the differential amplifier owe a lot to the range of results that can be obtained. The impedance parameters of the various pairs of probes should definitely match so as to avoid any interference in the differential drop applied across the Op-Amps. Here was, part of an attempt to study parasitic parameters, a motive to measure them and an expression for the need to minimize them as far as possible.

7. References

[1] Dennis Sylvester, James Chen, Chenming Hui; "Charge based Capacitance Measurement Technique", IEEE Custom Integrated Circuits Conference,1997.

[2] Hiroshi Iwai, Susumau Kohyama; On-Chip Measurement in VLSI Structures", IEEE Transactions on Electron Devices,Vol.ED-29,No.10,Oct.'82.

[3] "On chip Quasi-Static Floating Gate capacitance" : C.Kortekaas, Proc. IEEE 1990.Int. Conference on Microelectronic Test Structures,Vol.3 March '90

[4] Chi-Taou Tsai : "Package Inductance Characterization of High Frequencies", IEEE Trans on Components, Packaging and Manufacturing Technology PartB: Vol.17,No.2,May '94

[5] Charles E. Abernethy, John Prince; "Measuring Microelectronic Interconnect Transmission Parameters and Discontinuity Equivalent Electrical Parameters using Multiple Reflections", IEEE Trans on Components, Packaging and Manufacturing Tech. Part B: Vol. 19, '96.

[6] The Feynman Lectures on Physics: Feynman 2nd Volume

[7] Van der Pauw," Measurement of Resistivity on Lamellae of Arbitrary Shape", Philips Res. Reports.13,1958.

Figure 3 : Schematic diagram for Test Signal Injection Method

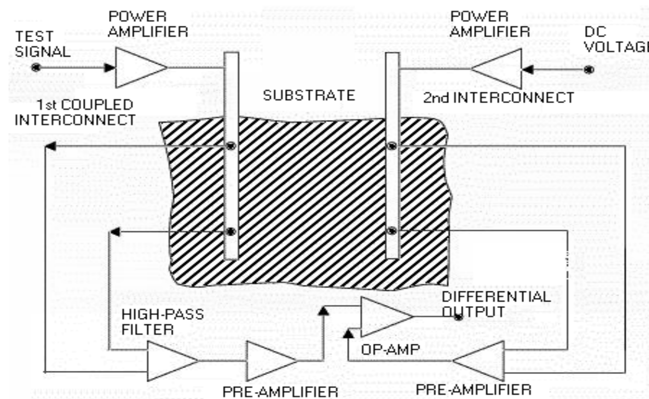


Figure 4 : On-Chip SPICE model of Test Signal Injection Method